

Advanced Computer Architecture

Lecture 1

Review of Basic Computer Organization



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Instruction Execution Cycle

<i>Instruction Fetch</i>
<i>Instruction Decode</i>
<i>Operand Fetch</i>
<i>Execute</i>
<i>Result Store</i>
<i>Next Instruction</i>

Obtain instruction from program storage

Determine required actions and instruction size

Locate and obtain operand data

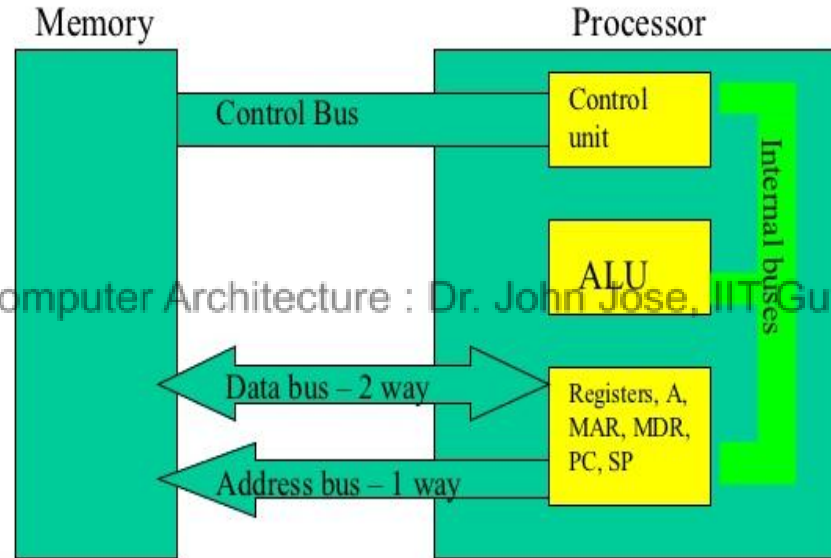
Compute result value or status

Deposit results in storage for later use

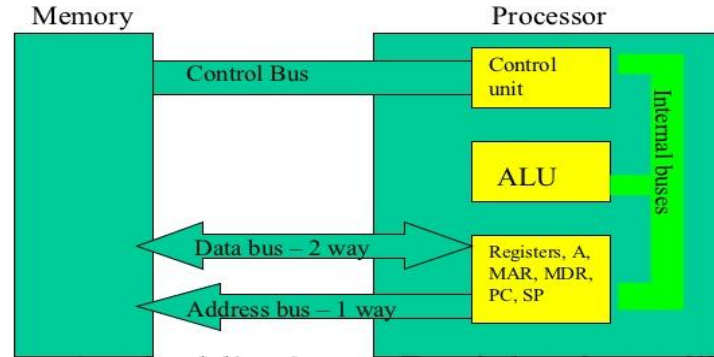
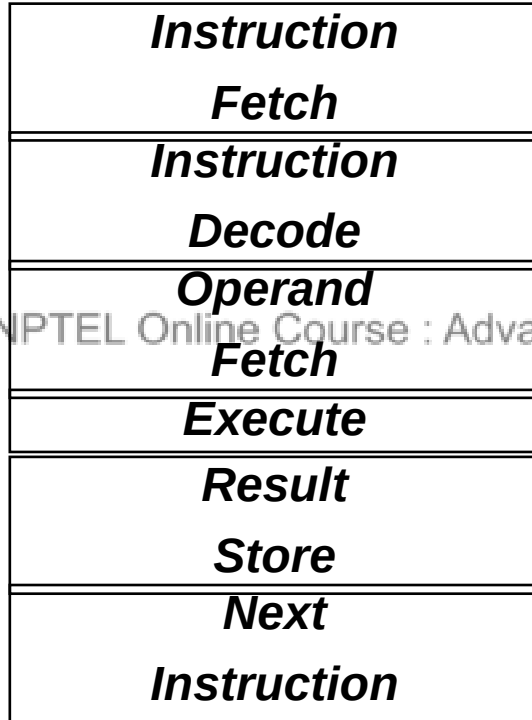
Determine successor instruction

Processor Memory Interaction

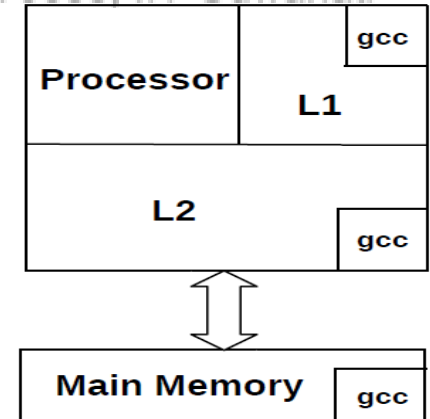
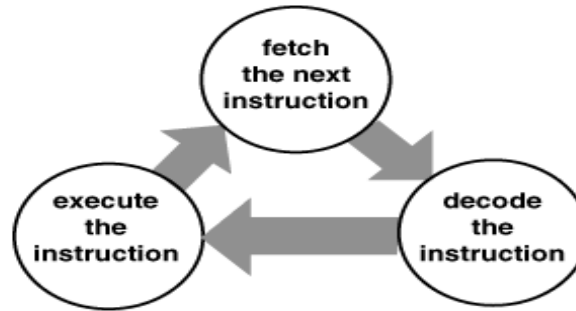
<i>Instruction Fetch</i>
<i>Instruction Decode</i>
<i>Operand Fetch</i>
<i>Execute</i>
<i>Result Store</i>
<i>Next Instruction</i>



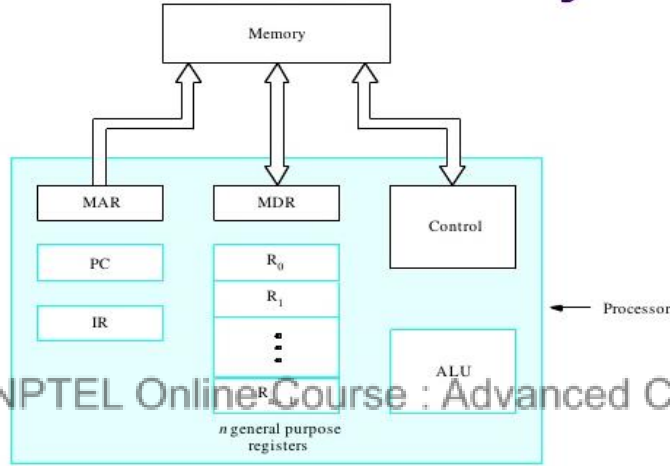
Processor Memory Interaction



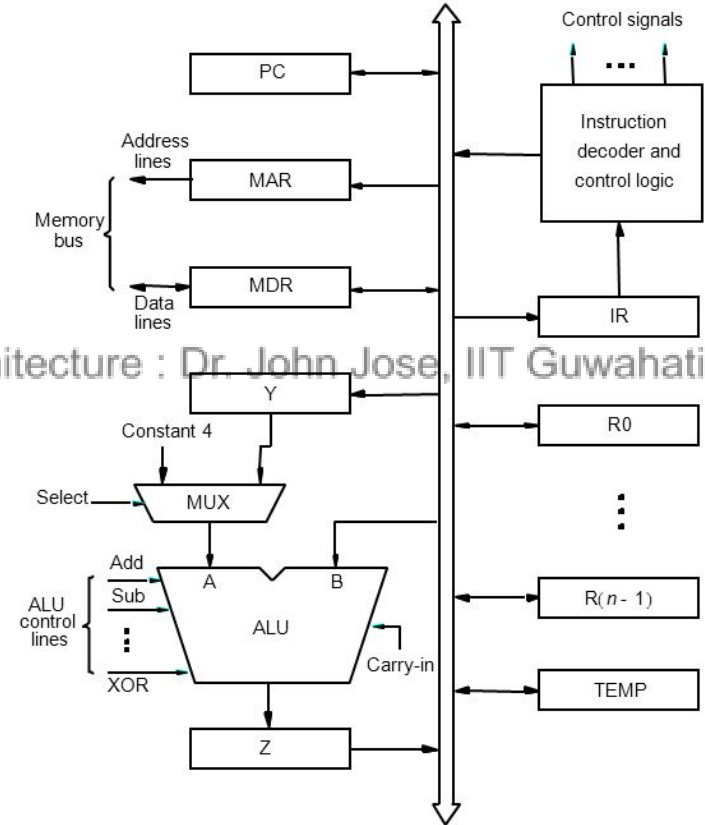
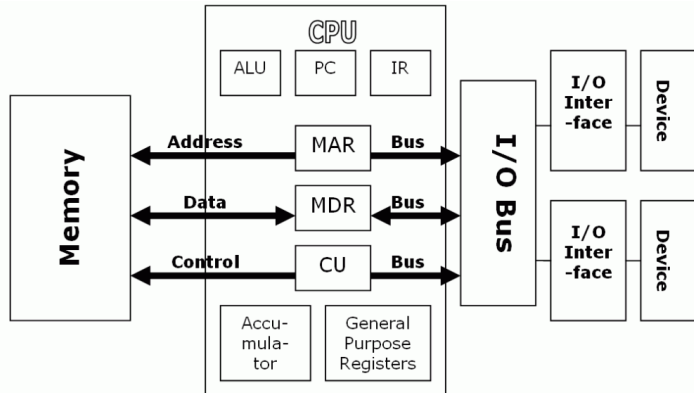
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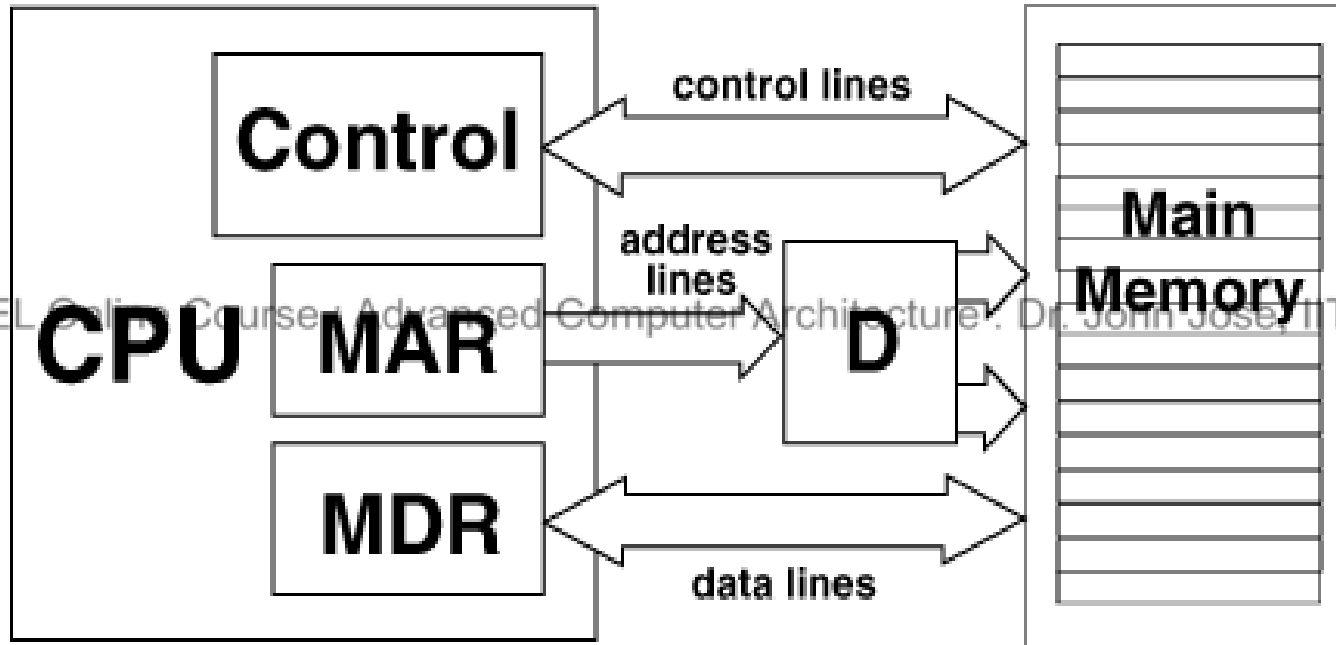
Processor Memory Interaction



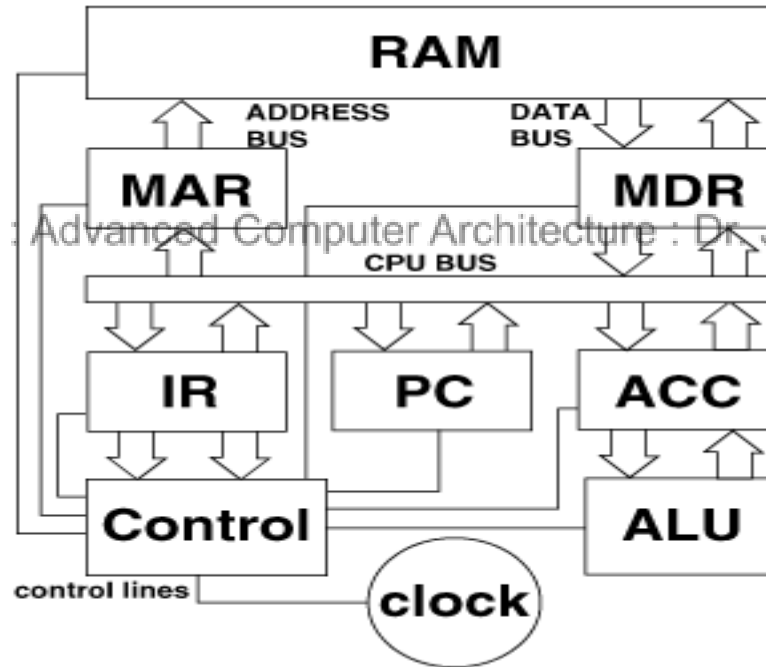
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Processor Memory Interaction



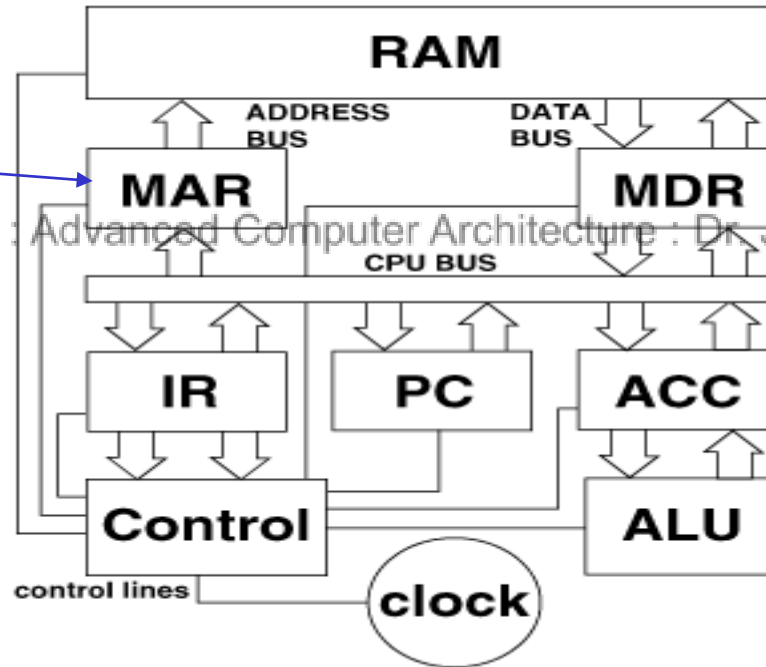
Inside the CPU



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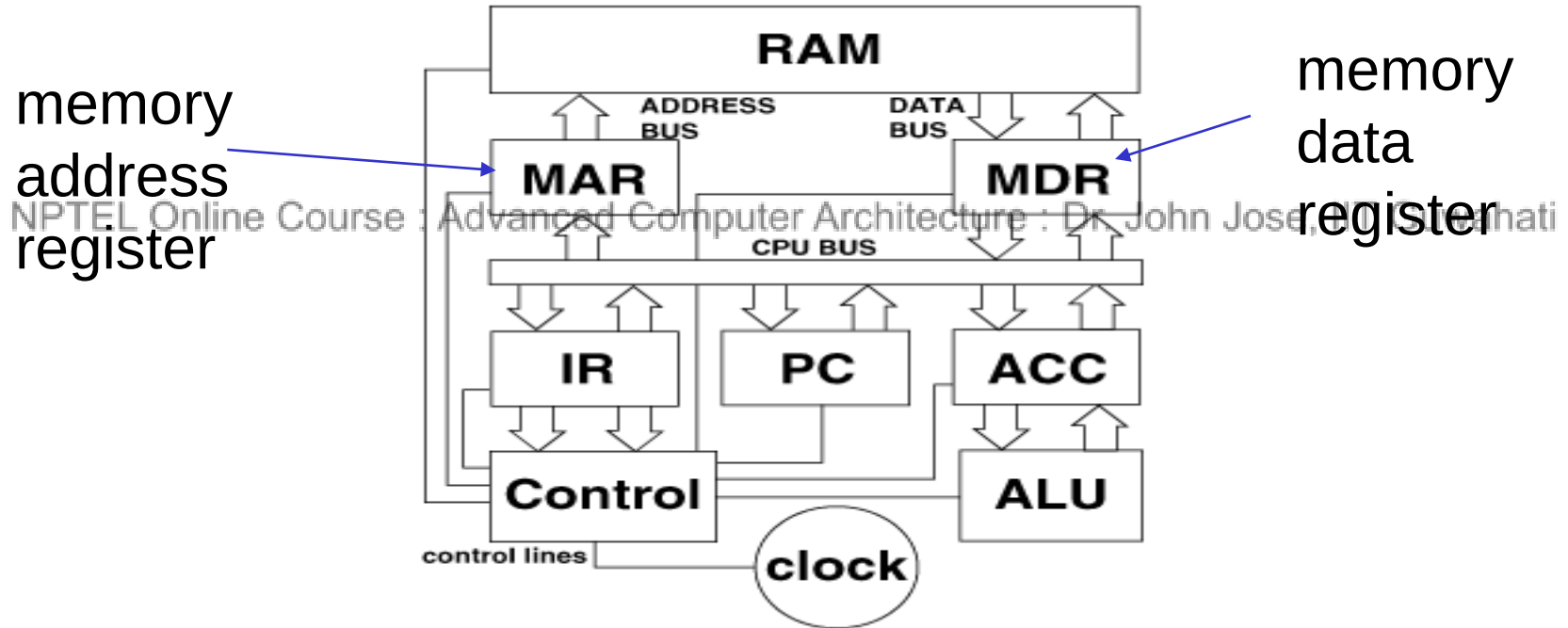
Inside the CPU

memory
address
register

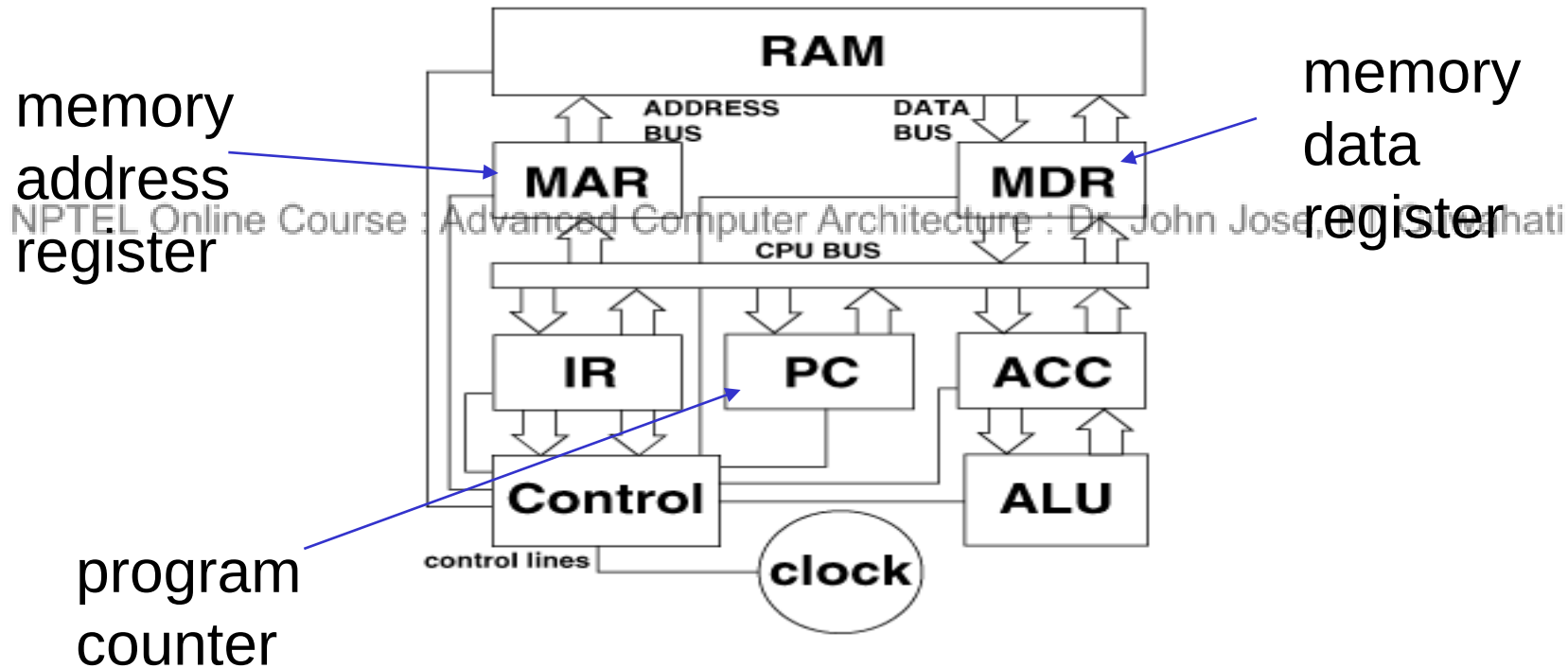


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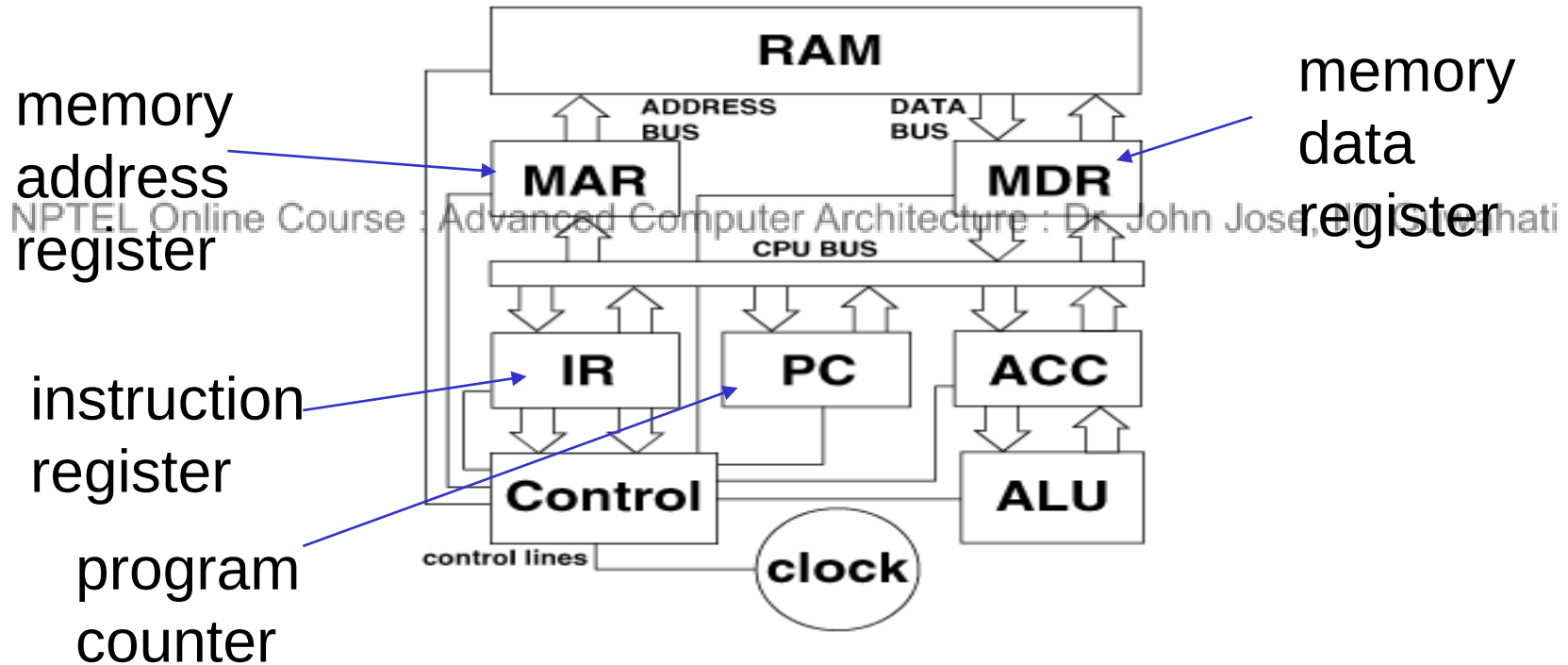
Inside the CPU



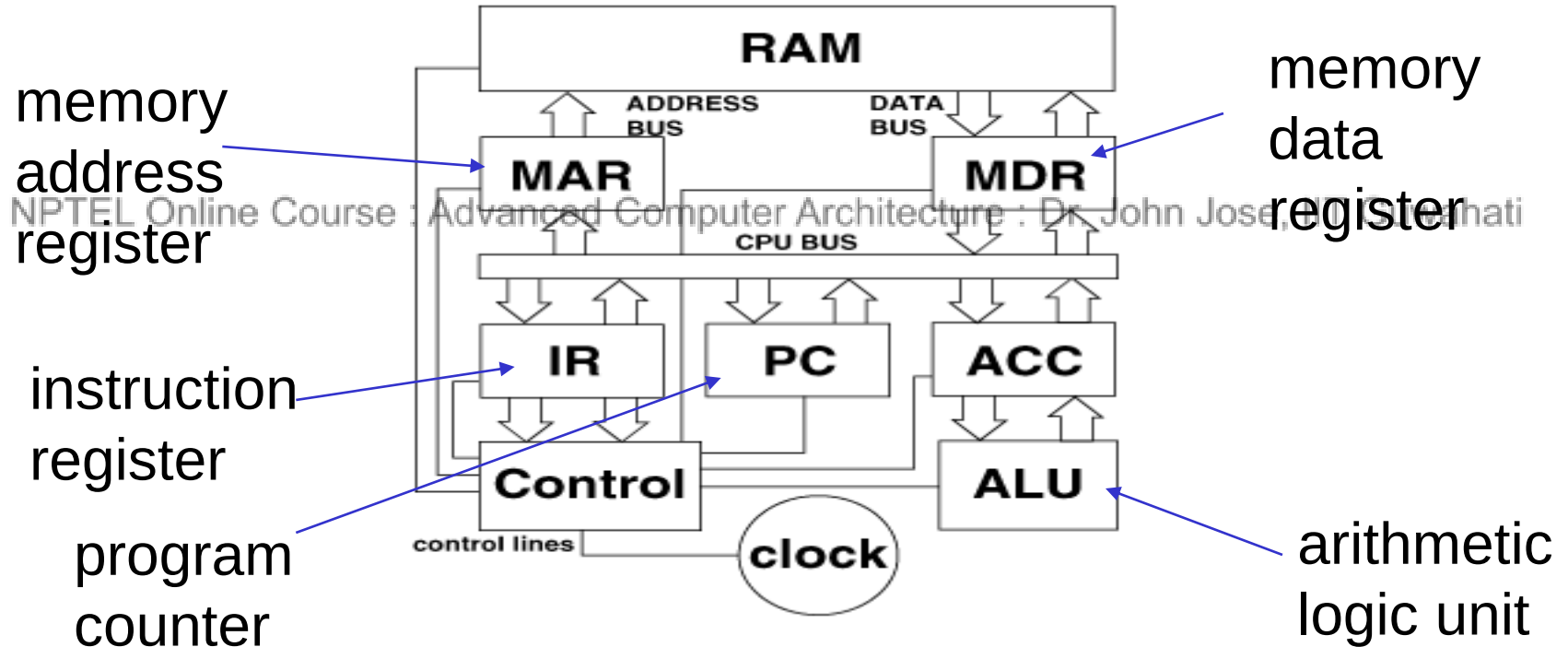
Inside the CPU



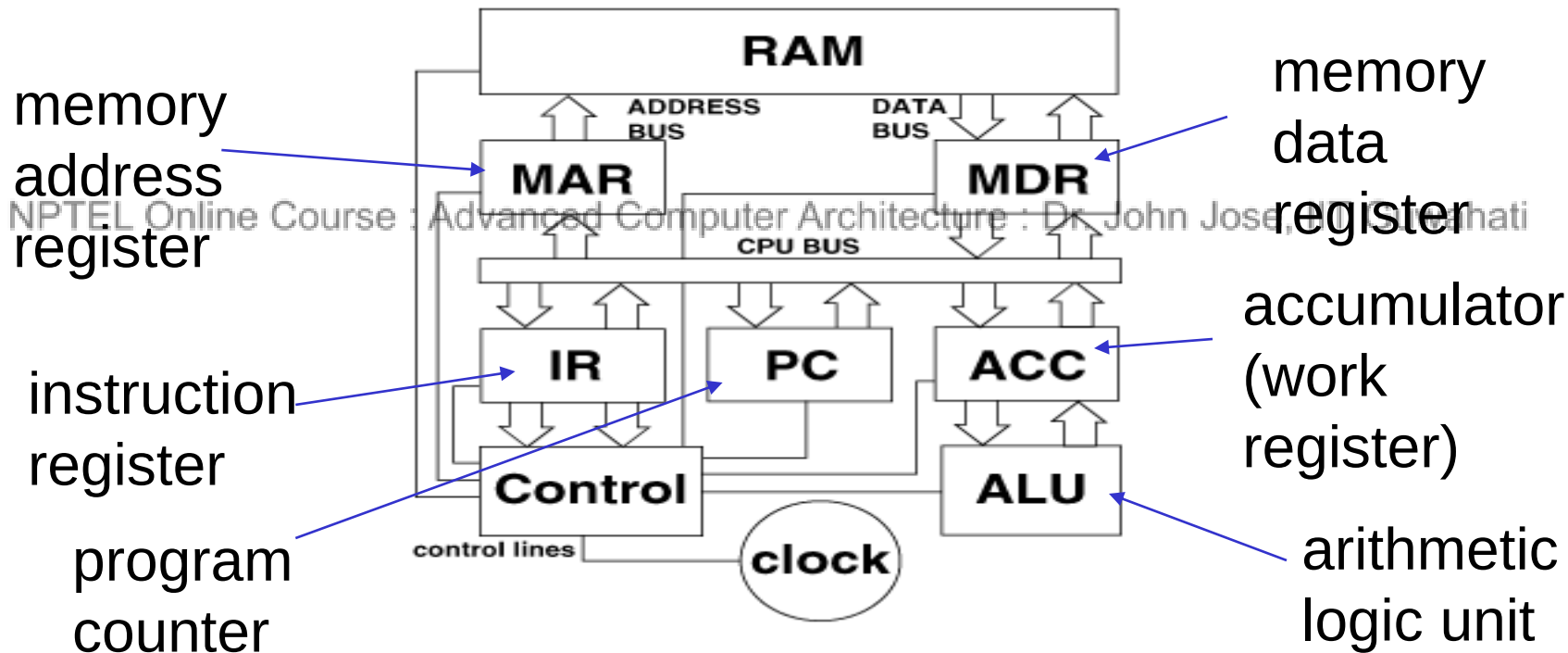
Inside the CPU



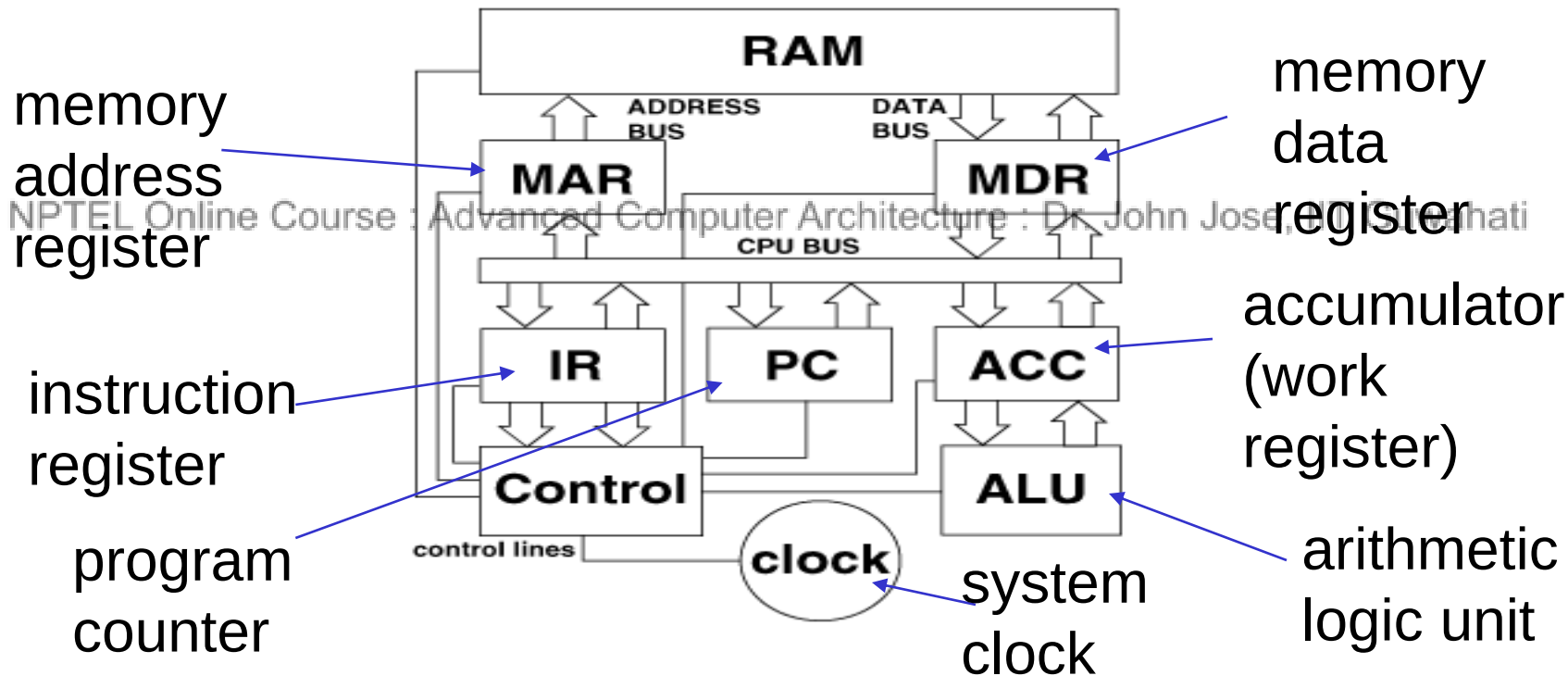
Inside the CPU



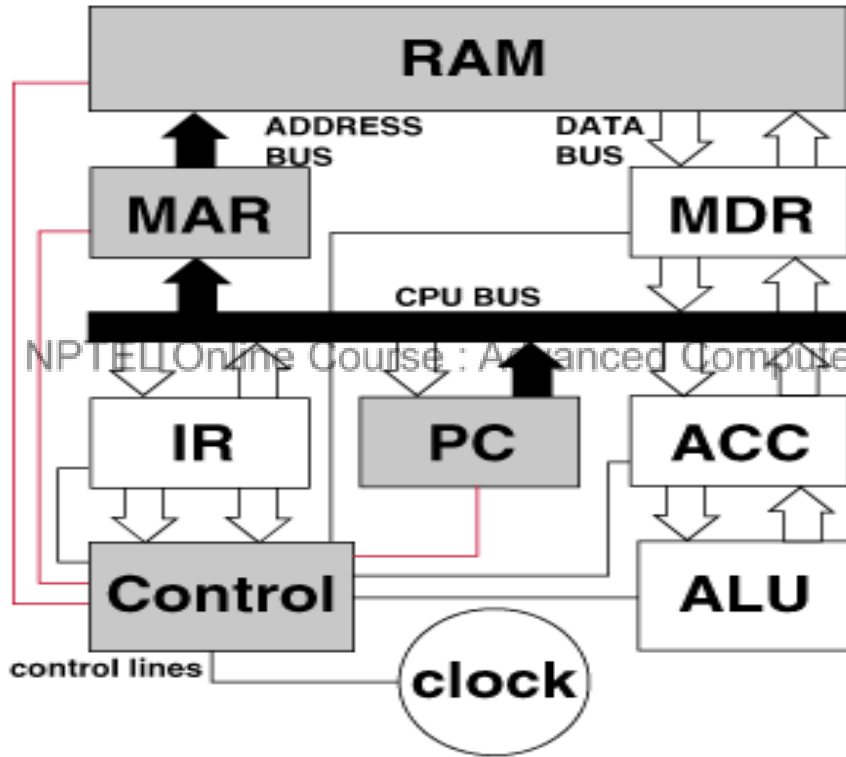
Inside the CPU



Inside the CPU



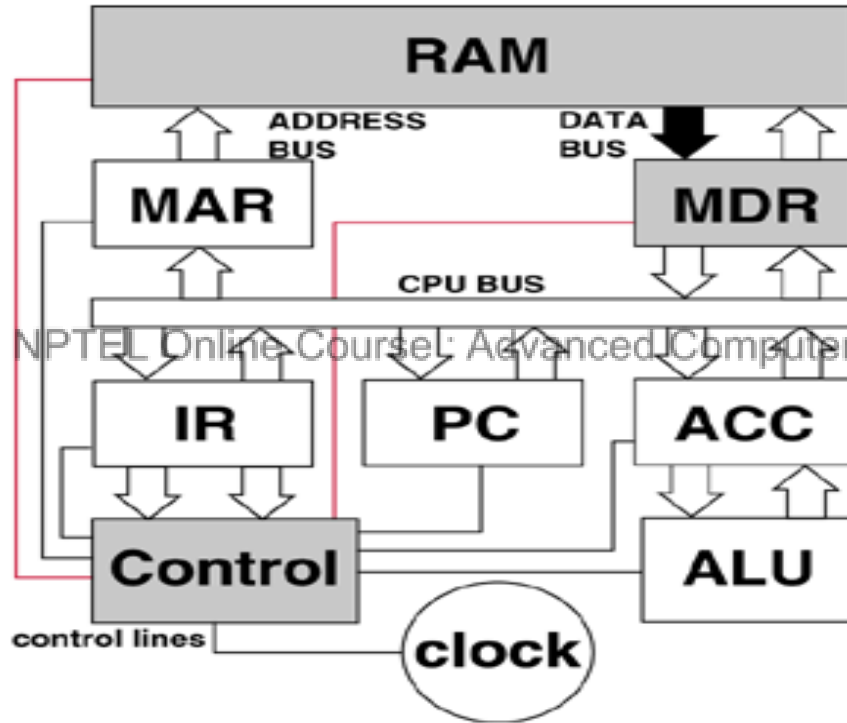
FETCH the instruction



1. address of the next instruction is transferred from PC to MAR

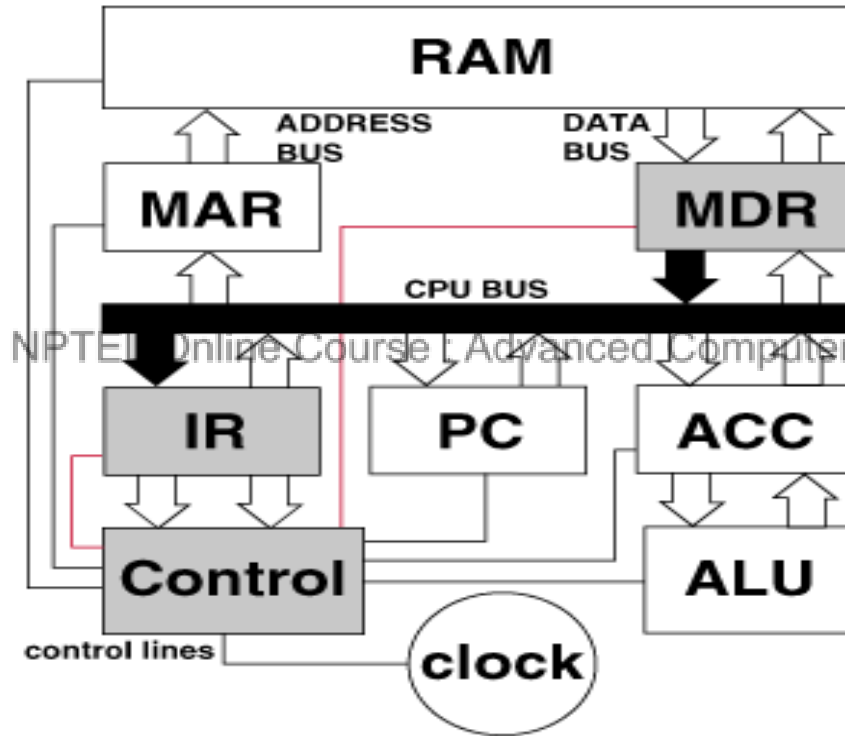
2. the instruction is located in memory

FETCH the instruction



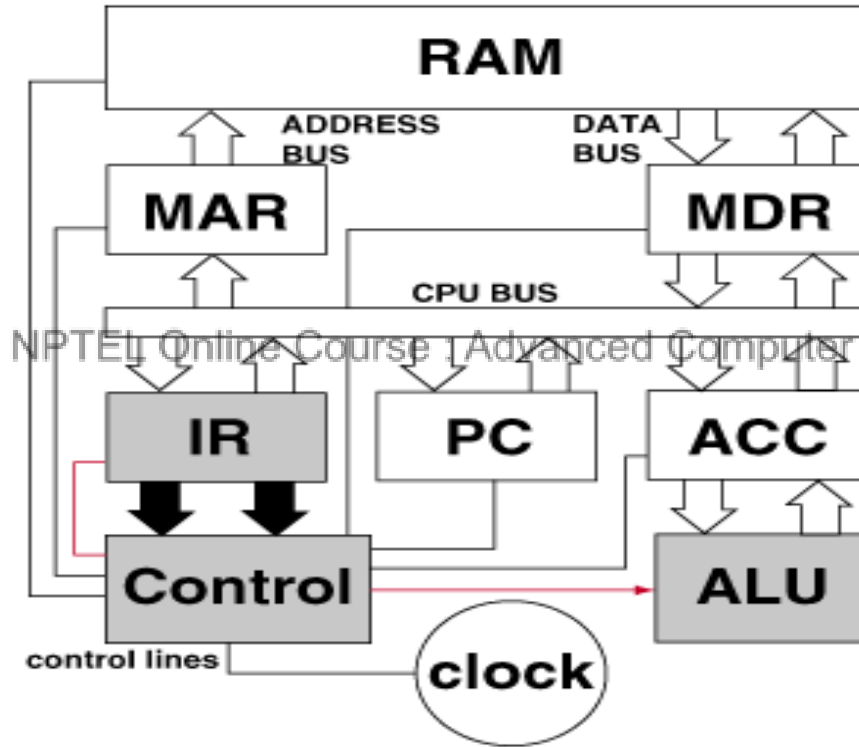
3. instruction is copied
from memory to MDR

DECODE the instruction



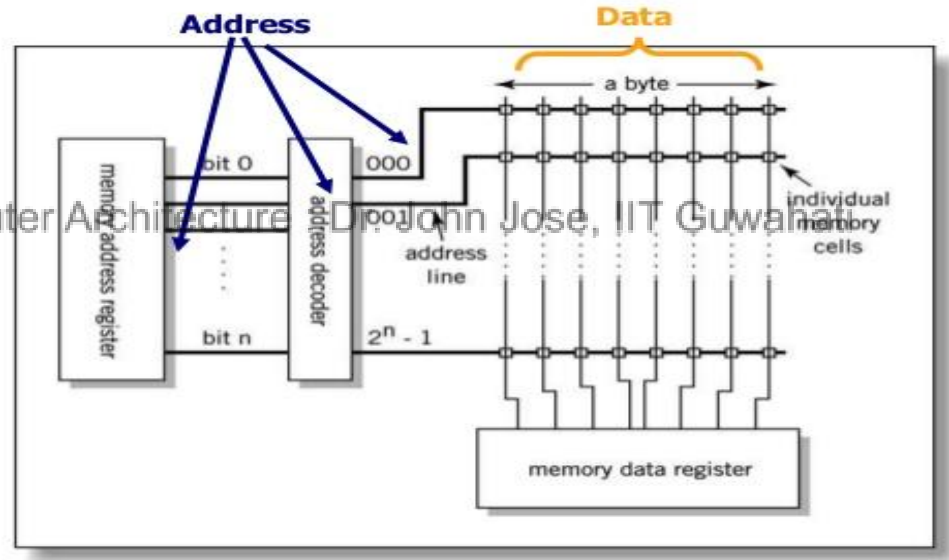
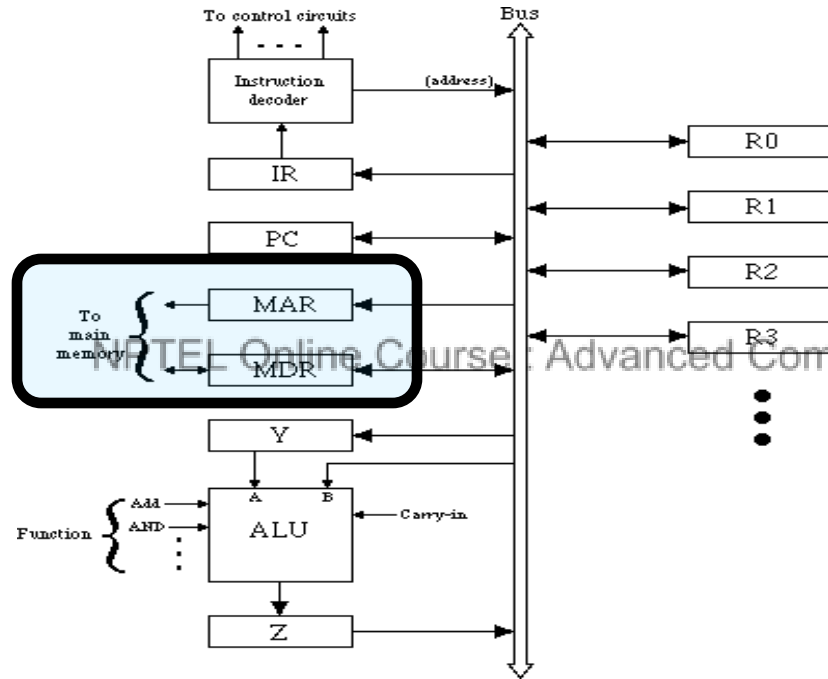
4. instruction is transferred to and decoded in the IR

EXECUTE the instruction

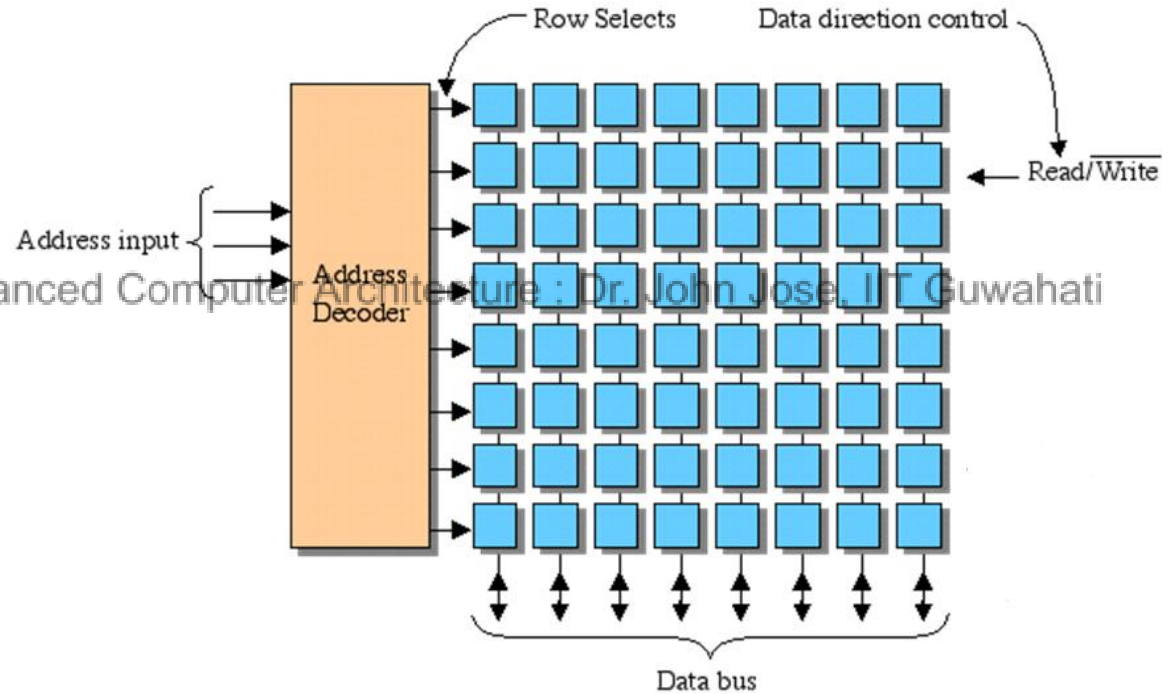
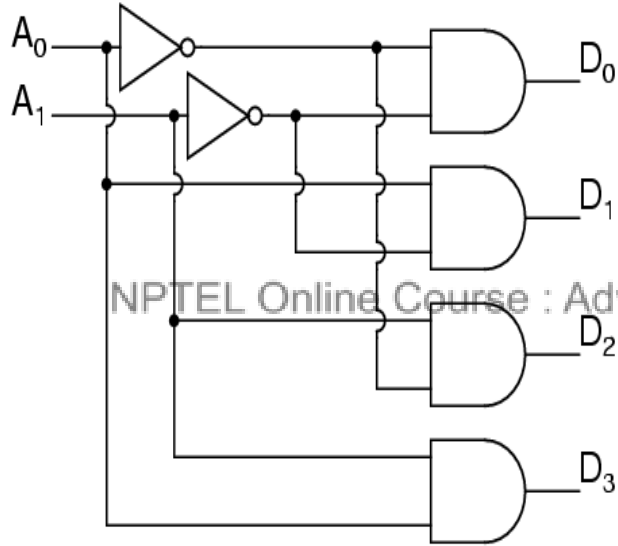


5. control unit sends signals to appropriate devices to cause execution of the instruction

Processor Memory Interaction

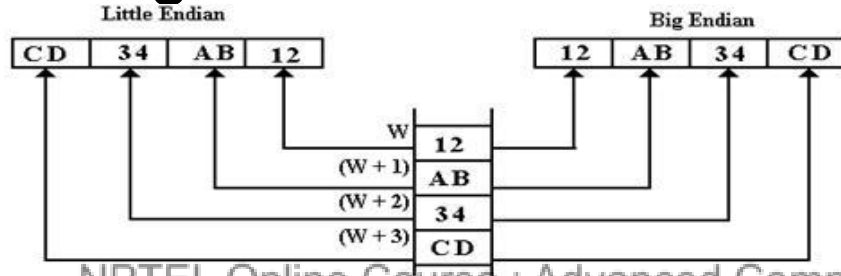


How memory works ?



Byte Ordering

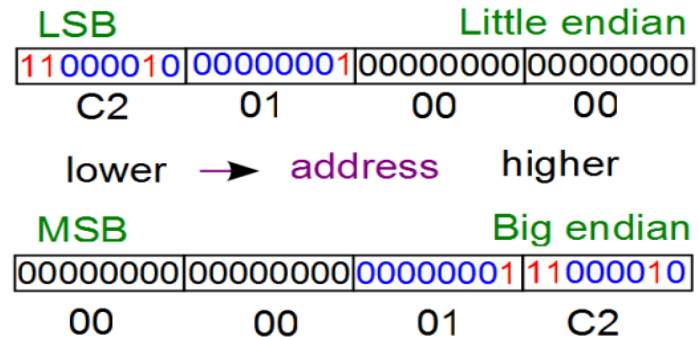
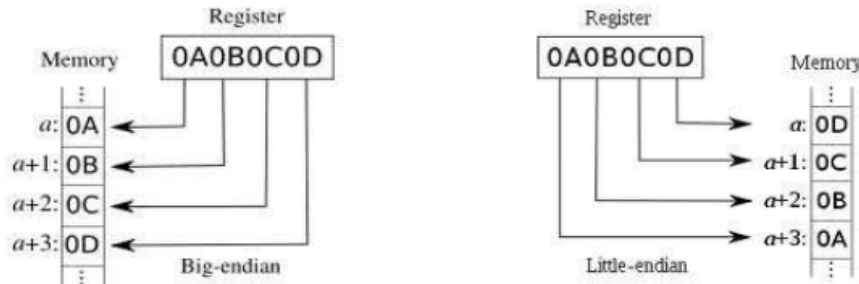
❖ Big Endian vs Little Endian



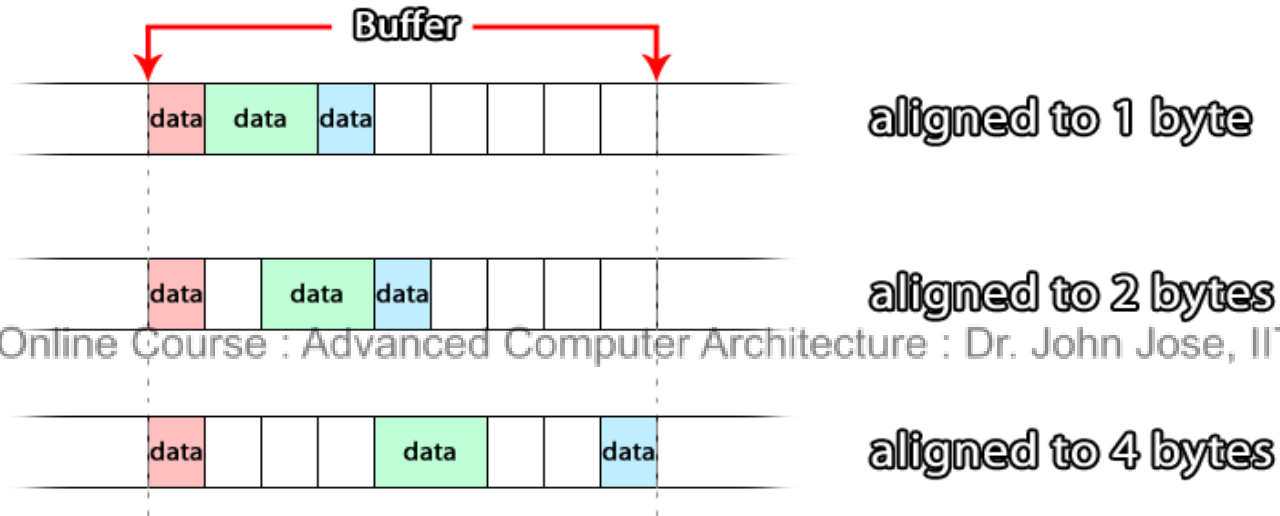
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Big Endian vs. Little Endian

$$\text{Int } i = 450 = 2^8 + 2^7 + 2^6 + 2 = \text{x000001C2}$$



Byte / Word Alignment



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Byte /Word Alignment

Value of 3 low-order bits of byte address								
Width of object	0	1	2	3	4	5	6	7
1 byte (byte)	Aligned	Aligned	Aligned	Aligned	Aligned	Aligned	Aligned	Aligned
2 bytes (half word)	Aligned		Aligned		Aligned		Aligned	
2 bytes (half word)		Misaligned		Misaligned		Misaligned		Misaligned
4 bytes (word)	Aligned				Aligned			
4 bytes (word)		Misaligned				Misaligned		
4 bytes (word)		Misaligned					Misaligned	
4 bytes (word)		Misaligned						Misaligned
8 bytes (double word)	Aligned							
8 bytes (double word)		Misaligned						
8 bytes (double word)		Misaligned						
8 bytes (double word)		Misaligned						
8 bytes (double word)		Misaligned						
8 bytes (double word)		Misaligned						
8 bytes (double word)		Misaligned						
8 bytes (double word)		Misaligned						
8 bytes (double word)		Misaligned						
8 bytes (double word)		Misaligned						

Types of Processor Operations

- ❖ Arithmetic and Logical Operations

- ❖ integer arithmetic

- ❖ comparing two quantities

- ❖ shifting, rotating bits in a quantity

- ❖ testing, comparing, and converting bits

Types of Processor Operations

❖ Data Movement Operations

- ❖ moving data from memory to the CPU
- ❖ moving data from memory to memory

❖ input and output

Types of Processor Operations

❖ Program Control Operations

- ❖ starting a program

- ❖ halting a program

- ❖ skipping to other instructions

- ❖ testing data to decide whether to skip over some instructions

Instruction Set Architecture

- ❖ Instruction vs Program vs Software

- ❖ Opcode, Operand

- ❖ Classification of ISA

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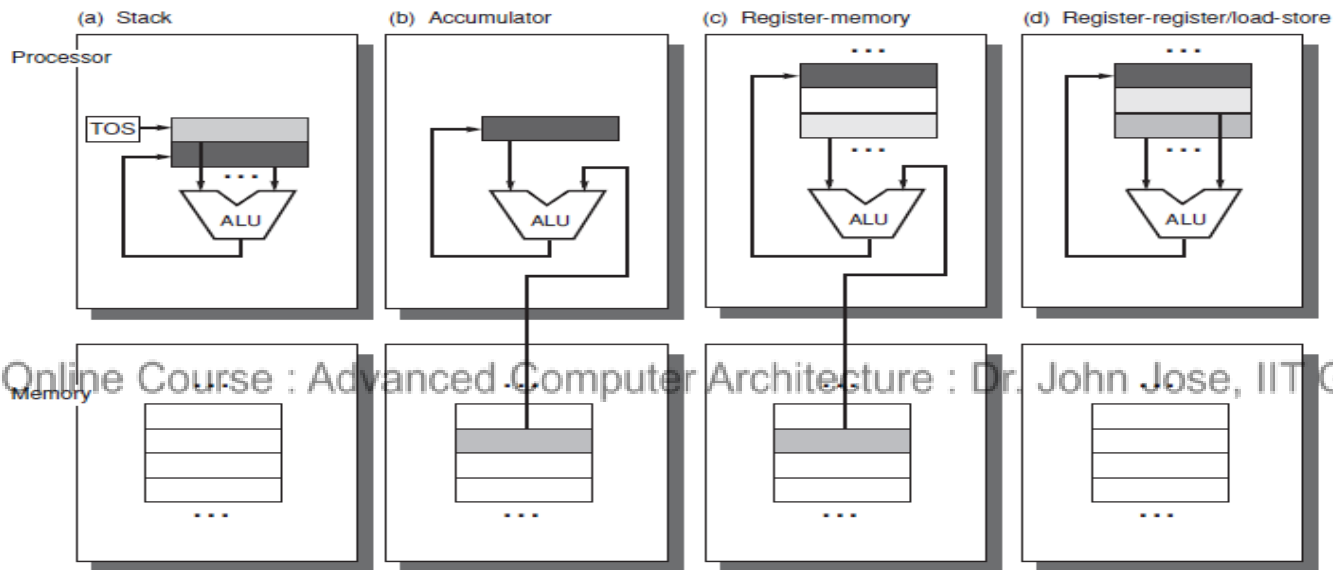
- ❖ Stack architecture

- ❖ Accumulator architecture

- ❖ Register-Memory architecture

- ❖ Register-Register/Load Store architecture

Instruction Set Architecture



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Stack	Accumulator	Register (register-memory)	Register (load-store)
Push A	Load A	Load R1,A	Load R1,A
Push B	Add B	Add R3,R1,B	Load R2,B
Add	Store C	Store R3,C	Add R3,R1,R2
Pop C			Store R3,C

The code sequence for $C = A + B$ for four classes of instruction sets.

Instruction Set Architecture

❖ $A = D * (B + C) - E$

Accumulator machine

Load Store machine

Stack machine

❖ Push D

❖ Push B

❖ Push C

❖ Add

❖ Mul

❖ Push E

❖ Sub

❖ Pop A

❖ Load B

❖ Add C

❖ Mul D

❖ Sub E

❖ Store A

❖ Load R1, D

❖ Load R2, B

❖ Load R3, C

❖ Add R4, R2, R3

❖ Mul R5, R1, R4

❖ Load R6, E

❖ Sub R7, R5, R6

❖ Store R7, A

Addressing Modes

❖ The way by which an operand is specified in an instruction.

– Register	<code>add r1, r2</code>	<code>r1 <- r1+r2</code>
– Immediate	<code>add r1, #5</code>	<code>r1 <- r1+5</code>
– Direct	<code>add r1, (0x200)</code>	<code>r1 <- r1+M[0x200]</code>
– Register indirect	<code>add r1, (r2)</code>	<code>r1 <- r1+M[r2]</code>
– Displacement	<code>add r1, 100(r2)</code>	<code>r1 <- r1+M[r2+100]</code>
– Indexed	<code>add r1, (r2+r3)</code>	<code>r1 <- r1+M[r2+r3]</code>
– Scaled	<code>add r1, (r2+r3*4)</code>	<code>r1 <- r1+M[r2+r3*4]</code>
– Memory indirect	<code>add r1, @(r2)</code>	<code>r1 <- r1+M[M[r2]]</code>
– Auto-increment	<code>add r1, (r2)+</code>	<code>r1 <- r1+M[r2], r2++</code>
– Auto-decrement	<code>add r1, -(r2)</code>	<code>r2--, r1 <- r1+M[r2]</code>

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**THANK
YOU!**

**FOR
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PRESENCE**

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